UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,891	08/11/2004	Yuan-Ting Wu	MTKP0088USA	4890

27765 7590 06/21/2007

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER
THAMMAVONG, PRASITH

ART UNIT	PAPER NUMBER
2187	

NOTIFICATION DATE	DELIVERY MODE
06/21/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

winstonhsu.uspto@gmail.com
Patent.admin.uspto.Rcv@naipo.com
mis.ap.uspto@naipo.com.tw

Office Action Summary	Application No.	Applicant(s)	
	10/710,891	WU ET AL.	
	Examiner	Art Unit	
	Prasith Thammavong	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The Examiner acknowledges the applicant's submission of the amendment dated 4/10/07. At this point, claim 22 have been added. Thus, claims 1-22 are pending in the instant application.

The instant application having Application No. 10/710,891 has a total of 22 claims pending in the application, there are 3 independent claims and 19 dependent claims, all of which are ready for examination by the examiner.

1. INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. ' 1.63**.

2. STATUS OF CLAIM FOR PRIORITY IN THE APPLICATION

As required by **M.P.E.P. ' 201.14(c)**, acknowledgment is made of applicant's claim for priority based on an application filed 9/2/03 in Taiwan.

3. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC ' 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 5-11, 13, 15-17, 19-22 are rejected under 35 U.S.C. 103(a) as

being unpatentable over Kaiser et al. (US Patent #5,784,710) in view of Hasbun (US Patent # 6,205,458).

With respect to claim 1, the Kaiser reference teaches a method for accessing a memory to protect a memory section from being accessed or changed incorrectly when accessing the memory:

generating a first logic address data (figure 2, Address (n-m));

selectively outputting the first logic address data or a second logic address data (fig. 2, input 1 of mux 205) as a physical address data (fig. 2, new address (n-m)) by using an address translator (fig. 2, element 20) according to a control signal (fig. 2, select line) (column 3, line 63 to column 4, line 24, where the mux 205 outputs the new address (n-m) according to a select line and 2 addresses);

accessing the memory according to the physical address data; (column 4, lines 25-35)

wherein the second logic address data is a result obtained after operating on the first logic address data. (column 4, lines 9-20, where input 1 is determined after being ORed with the address (n-m) and address mask (n-m))

However, the Kaiser reference does not explicitly teach turning on the address translator utilizing the control signal so that the second logic address data is outputted as the physical address data when it is required to protect the memory section from being accessed;

The Hasbun reference teaches turning on the address translator utilizing the control signal so that the second logic address data is outputted as the physical address

data when it is required to protect the memory section from being accessed (column 6, lines 31-50, where the boot selector can choose which portion to select to boot from and where the boot selector can be locked thus protecting it from inadvertent updating).

The Kaiser and Hasbun references are analogous art because they are in the same field of endeavor of memory access and control.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the Kaiser reference to turn on the address translator utilizing the control signal so that the second logic address data is outputted as the physical address data when it is required to protect the memory section from being accessed, which is taught by the Hasbun reference.

The suggestion/motivation for doing so would have been to prevent inadvertent updating of the currently selected boot block (Hasbun, column 6, lines 31-50).

Therefore it would have been obvious to combine the teachings of Kaiser reference with the Hasbun reference for the benefit of preventing inadvertent updating of the currently selected boot block to obtain the invention as specified in claim 1.

With respect to claim 2, the Kaiser reference teaches operating on the first logic address data by using the address translator according to a setup value (fig. 2, element 201) in order to generate the second logic address data (column 3 line 63 to column 4, line 20, where the Address Mask 201 is used to create input 1 of the mux).

With respect to claim 3, the Kaiser reference teaches the setup value is a value representing a characteristic of the memory section (column 4, lines 5-8).

With respect to claim 5, the Kaiser reference teaches the address translator further comprises an operating unit (see fig. 2, element 202), and the method further comprises operating on the first logic address data by using the operating unit according to the setup value to generate the second logic address data (column 3 line 63 to column 4, line 20, where the Address Mask 201 is ORed with the Address Mask (N-M) to create input 1 of the mux).

With respect to claim 6, the Kaiser reference teaches address translator further comprises a multiplexer (fig. 2, element 205), and the method further comprises multiplexing the first logic address data and the second logic address data by using the multiplexer to selectively output the first logic address data or the second logic address data (column 4, lines 9-20, where the circuitry uses the mux to select input 0 or 1).

With respect to claim 7, the Kaiser reference teaches a microprocessor system for accessing a memory comprising:

a microprocessor (fig. 1, element 108) for providing a first logic address data (figure 2, Address (n-m));

a memory comprising a first memory section (fig. 1, element 105) and a second memory section (fig. 1, element 102); and

an address translator (fig. 1, element 20) coupled between the microprocessor and the memory to selectively output the first logic address data (see fig. 2, address (n-m)) or a second logic address data (fig. 2, input 1 of mux 205) as a physical address data (fig. 2, new address (n-m)) according to a control signal (fig. 2, select line); (column

3, line 63 to column 4, line 24, where the mux 205 outputs the new address (n-m) according to a select line and 2 addresses)

and the second logic address data is a result obtained after operating on the first logic address data and the microprocessor accesses data of the first memory section or the second memory section according to the physical address data (column 4, lines 9-20, where input 1 is determined after being ORed with the address (n-m) and address mask (n-m) and column 4, lines 25-35).

However, the Kaiser reference does not explicitly teach turning on the address translator utilizing the control signal so that the second logic address data is outputted as the physical address data when it is required to protect the first memory section from being accessed.

The Hasbun reference teaches turning on the address translator utilizing the control signal so that the second logic address data is outputted as the physical address data when it is required to protect the first memory section from being accessed (column 6, lines 31-50, where the boot selector can choose which portion to select to boot from and where the boot selector can be locked thus protecting it from inadvertent updating).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the Kaiser reference to turn on the address translator utilizing the control signal so that the second logic address data is outputted as the physical address data when it is required to protect the first memory section from being accessed, which is taught by the Hasbun reference.

The suggestion/motivation for doing so would have been to prevent inadvertent updating of the currently selected boot block (Hasbun, column 6, lines 31-50).

Therefore it would have been obvious to combine the teachings of Kaiser reference with the Hasbun reference for the benefit of preventing inadvertent updating of the currently selected boot block to obtain the invention as specified in claim 7.

With respect to claim 8, the Kaiser reference teaches the memory is a non-volatile memory (see fig. 2, elements 104 and 105).

With respect to claim 9, the Kaiser reference teaches the address translator operates the first logic address data according to a setup value (fig. 2, element 201) to generate the second logic address data (column 3 line 63 to column 4, line 20, where the Address Mask 201 is used to create input 1 of the mux).

With respect to claim 10, the Kaiser reference teaches the setup value is a value representing a characteristic of the first memory section. (column 4, lines 5-8)

With respect to claim 11, the Kaiser reference teaches the address translator further comprises an operating unit to operate the first logic address data according to the setup value in order to generate the second logic address data (column 3 line 63 to column 4, line 20, where the Address Mask 201 is ORed with the Address Mask (N-M) to create input 1 of the mux).

With respect to claim 13, the Kaiser reference teaches address translator further comprises a multiplexer for multiplexing the first logic address data and the second logic address data in order to selectively output the first logic address data or

the second logic address data. (column 4, lines 9-20, where the address translator uses the mux to select input 0 or 1).

With respect to claim 15, the Kaiser reference teaches the memory section comprises boot code (see fig. 2, element 105) for a microprocessor, the microprocessor for generating the first logic address data. (column 3, lines 44-51, where the processor provides an address for the IPL code)

With respect to claim 16, the Kaiser reference does not explicitly teach:

turning off the address translator utilizing the control signal so that the first logic address data is outputted as the physical address data when power is turned on or restored to the microprocessor to thereby allow access to the boot code; and

when the microprocessor has successfully booted the system according to the boot code, turning on the address translator utilizing the control signal so that the second logic address data is outputted as the physical address data to thereby protect the boot code from being accessed.

However, the Hasbun reference does teach:

turning off the address translator utilizing the control signal so that the first logic address data is outputted as the physical address data when power is turned on or restored to the microprocessor to thereby allow access to the boot code (column 7, lines 3-13, where the boot selector allows access to the boot code); and

when the microprocessor has successfully booted the system according to the boot code, turning on the address translator utilizing the control signal so that the second logic address data is outputted as the physical address data to thereby protect the boot code from being accessed (column 7, lines 3-13, where the boot selector does not allow access to the boot code).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the Kaiser reference to turn off the address translator utilizing the control signal so that the first logic address data is outputted as the physical address data when power is turned on or restored to the microprocessor to thereby allow access to the boot code; and when the microprocessor has successfully booted the system according to the boot code, turning on the address translator utilizing the control signal so that the second logic address data is outputted as the physical address data to thereby protect the boot code from being accessed, which is taught by the Hasbun reference.

The suggestion/motivation for doing so would have been to prevent inadvertent updating of the currently selected boot block (Hasbun, column 6, lines 31-50).

Therefore it would have been obvious to combine the teachings of Kaiser reference with the Hasbun reference for the benefit of preventing inadvertent updating of the currently selected boot block to obtain the invention as specified in claim 16.

With respect to claim 17, the Kaiser reference does not explicitly teach:

turning off the address translator utilizing the control signal so that the first logic address data is outputted as the physical address data when it is required to erase or

update the boot code to thereby allow access to the boot code in the memory section by the microprocessor.

However, the Hasbun reference does teach turning off the address translator utilizing the control signal so that the first logic address data is outputted as the physical address data when it is required to erase or update the boot code to thereby allow access to the boot code in the memory section by the microprocessor (column 7, lines 3-13, where the boot selector allows the portion not selected to have its boot code updated).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the Kaiser reference to turn off the address translator utilizing the control signal so that the first logic address data is outputted as the physical address data when it is required to erase or update the boot code to thereby allow access to the boot code in the memory section by the microprocessor, which is taught by the Hasbun reference.

The suggestion/motivation for doing so would have been to prevent inadvertent updating of the currently selected boot block and allow updating to the non-selected portion (Hasbun, column 6, lines 31-50).

Therefore it would have been obvious to combine the teachings of Kaiser reference with the Hasbun reference for the benefit of preventing inadvertent updating of the currently selected boot block allow updating to the non-selected portion to obtain the invention as specified in claim 16.

With respect to claim 19, the Kaiser reference teaches the memory section comprises boot code for a microprocessor (see fig. 2, element 105), the microprocessor for generating the first logic address data. (column 3, lines 44-51, where the processor provides an address for the IPL code)

With respect to claim 20, the Kaiser reference does not explicitly teach:

turning off the address translator utilizing the control signal so that the first logic address data is outputted as the physical address data when power is turned on or restored to the microprocessor to thereby allow access to the boot code; and

when the microprocessor has successfully booted the system according to the boot code, turning on the address translator utilizing the control signal so that the second logic address data is outputted as the physical address data to thereby protect the boot code from being accessed.

However, the Hasbun reference does teach:

turning off the address translator utilizing the control signal so that the first logic address data is outputted as the physical address data when power is turned on or restored to the microprocessor to thereby allow access to the boot code (column 7, lines 3-13, where the boot selector allows access to the boot code); and

when the microprocessor has successfully booted the system according to the boot code, turning on the address translator utilizing the control signal so that the second logic address data is outputted as the physical address data to thereby protect

the boot code from being accessed (column 7, lines 3-13, where the boot selector does not allow access to the boot code).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the Kaiser reference to turn off the address translator utilizing the control signal so that the first logic address data is outputted as the physical address data when power is turned on or restored to the microprocessor to thereby allow access to the boot code; and when the microprocessor has successfully booted the system according to the boot code, turning on the address translator utilizing the control signal so that the second logic address data is outputted as the physical address data to thereby protect the boot code from being accessed, which is taught by the Hasbun reference.

The suggestion/motivation for doing so would have been to prevent inadvertent updating of the currently selected boot block (Hasbun, column 6, lines 31-50).

Therefore it would have been obvious to combine the teachings of Kaiser reference with the Hasbun reference for the benefit of preventing inadvertent updating of the currently selected boot block to obtain the invention as specified in claim 16.

With respect to claim 21, the Kaiser reference does not explicitly teach:

turning off the address translator utilizing the control signal so that the first logic address data is outputted as the physical address data when it is required to erase or update the boot code to thereby allow access to the boot code in the first memory section by the microprocessor.

However, the Hasbun reference does teach turning off the address translator utilizing the control signal so that the first logic address data is outputted as the physical address data when it is required to erase or update the boot code to thereby allow access to the boot code in the first memory section by the microprocessor (column 7, lines 3-13, where the boot selector allows the portion not selected to have its boot code updated).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the Kaiser reference to turn off the address translator utilizing the control signal so that the first logic address data is outputted as the physical address data when it is required to erase or update the boot code to thereby allow access to the boot code in the first memory section by the microprocessor, which is taught by the Hasbun reference.

The suggestion/motivation for doing so would have been to prevent inadvertent updating of the currently selected boot block and allow updating to the non-selected portion (Hasbun, column 6, lines 31-50).

Therefore it would have been obvious to combine the teachings of Kaiser reference with the Hasbun reference for the benefit of preventing inadvertent updating of the currently selected boot block allow updating to the non-selected portion to obtain the invention as specified in claim 16.

With respect to claim 22, the Kaiser reference teaches a method for protecting a memory section from being accessed, the method comprising:

generating a first logic address data; (figure 2, Address (n-m));

selectively outputting the first logic address data or a second logic address data (fig. 2, input 1 of mux 205) as a physical address data (fig. 2, new address (n-m)) by using an address translator (fig. 2, element 20) according to a control signal (fig. 2, select line) (column 3, line 63 to column 4, line 24, where the mux 205 outputs the new address (n-m) according to a select line and 2 addresses);

accessing the memory according to the physical address data; (column 4, lines 25-35)

wherein the second logic address data is a result obtained after operating on the first logic address data. (column 4, lines 9-20, where input 1 is determined after being ORed with the address (n-m) and address mask (n-m))

However, the Kaiser reference does not explicitly teach protecting the memory section from being accessed by outputting the second logic address data as the physical address data from the address translator when it is required to protect the memory section from being accessed.

The Hasbun reference teaches protecting the memory section from being accessed by outputting the second logic address data as the physical address data from the address translator when it is required to protect the memory section from being accessed. (column 6, lines 31-50, where the boot selector can choose which portion to select to boot from and where the boot selector can be locked thus protecting it from inadvertent updating).

The Kaiser and Hasbun references are analogous art because they are in the same field of endeavor of memory access and control.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the Kaiser reference to protect the memory section from being accessed by outputting the second logic address data as the physical address data from the address translator when it is required to protect the memory section from being accessed, which is taught by the Hasbun reference.

The suggestion/motivation for doing so would have been to prevent inadvertent updating of the currently selected boot block (Hasbun, column 6, lines 31-50).

Therefore it would have been obvious to combine the teachings of Kaiser reference with the Hasbun reference for the benefit of preventing inadvertent updating of the currently selected boot block to obtain the invention as specified in claim 1.

Claims 4, 12, 14 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Kaiser et al. (US Patent #5,784,710) and Hasbun (US Patent # 6,205,458) references as applied to claims 2, 5, 9 and 11 above, and further in view of Debruler (US Patent #4,539,637).

With respect to claim 14 and 18, the combination of the Kaiser and Hasbun references does not explicitly teach that the operating unit of the address translator is an adder.

However, the DeBruler reference does teach the operating unit of the address translator is an adder (see fig 2, element 320).

The Kaiser, Hasbun, and DeBruler references are analogous art because they are in the same field of endeavor of memory access and control.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the combination of the Kaiser and Husbun references for the operating unit of the address translate to be an adder, which is taught by the DeBruler reference.

The suggestion/motivation for doing so would have been to have flexibility on the way addresses are created from other data such as other addresses and offsets.

Therefore it would have been obvious to combine the combination of the Kaiser and Hasbun references with the DeBruler reference for the benefit of being able to create new addresses to obtain the invention as specified in claims 14 and 18.

With respect to claim 4 and 12, the combination of the Kaiser and Hasbun references does not explicitly teach that the setup value is stored in a register.

However, the DeBruler reference does teach the setup value is stored in a register (see fig 2, element 330).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the combination of the Kaiser and Hasbun references for the operating unit of the address translate to be an adder, which is taught by the DeBruler reference.

The suggestion/motivation for doing so would have been to have flexibility on where data, such as other addresses and offsets, could be stored.

Therefore it would have been obvious to combine the combination of the Kaiser and Hasbun references with the DeBruler reference for the benefit of being able to create new addresses to obtain the invention as specified in claims 4 and 12.

4. ARGUMENTS CONCERNING PRIOR ART REJECTIONS

Rejections - USC 102/103

Applicant's arguments with respect to claims 1-22 have been considered but are not persuasive.

With respect to arguments pertaining to claims 1-3, 5-11, 13, 15-17 and 19-21 on page 8, lines 9-13 which states:

In contrast to this claimed operation of the present invention, the cited references of Kaiser et al. and Hasbun do not teach translating address data according to a control signal and turning on the address translator according to the same control signal to thereby protect the boot code section from being accessed. Additionally, applicant further asserts there is no motivation provided by the cited references to suggest such an operation.

Applicant's arguments towards **claims 1-3, 5-11, 13, 15-17 and 19-21** have been considered, but the Examiner respectfully disagrees. The Examiner contends that the same control signal can be used as explained below in the next reply section. The Examiner also contends that the Hasbun reference does teach a motivation for the combining the references, which would be to prevent inadvertent updating of the currently selected boot block (Hasbun, column 6, lines 31-50).

With respect to arguments pertaining to claims1-3, 5-11, 13, 15-17 and 19-21 on page 9, lines 9-27 which states:

Therefore, applicant firstly asserts that combining the teachings of Kaiser et al. with Hasbun would not result in the present invention as claimed in claim 1 because the SELECT signal utilized to translate the address for a processor not having enough bits needed to access IPL code on boot-up would not be the same as the boot selector signal which would need to select which block in the volatile memory needs to be accessed in order for the processor to boot. The reason these two control signals need to be different is that Hasbun teaches selecting a particular boot code section in the non-volatile memory according to the block selector, which would need to be selected separately than the SELECT signal used to turn on the address translator if the output of the concatenating circuit 203 matches a target address range as taught by Kaiser et al. Simply put, a person skilled in the art would be motivated to use separate control signals in order to gain the benefit as taught by Hasbun of having two exclusively selectable boot code (sections 342 or 344 in Figure 3 by Hasbun) that could be accessed with processors (units 108 or 109 in Figure 1 of Kaiser el al.) as taught by Kaiser et at. In order to maintain the principle of

operation of the two cited references, the combination would require two independent control signals that are not the same. This is clearly different from the present invention as claimed in claim 1 because a single control signal is claimed in the present invention to turn on the address translator when it is required to protect the memory section from being accessed.

Applicant's arguments towards **claims 1-3, 5-11, 13, 15-17 and 19-21** have been considered, but the Examiner respectfully disagrees. The Examiner contends that the same control signal can be used in order to allow access to a certain area of memory as the control signal found in the Kaiser reference (column 4, lines 29-35) is meant to allow access to certain regions of memory. Additionally, the Hasbun reference teaches that the block selector's value is a binary number (column 5, line 44-51) just like the binary number of the select line in the Kaiser reference (fig. 2, select line; and column 4, lines 9-20) and thus could be utilized for the same purpose since they both allow access to certain portions of a memory.

With respect to arguments pertaining to claims 1-3, 5-11, 13, 15-17 and 19-21 on page 9, line 28 to page 10, line 10 which states:

Secondly, applicant asserts that combining the teachings of Kaiser et al. with Hasbun would not result in the present invention as claimed in claim 1 because Hasbun does not teach preventing taming on the address translator when it is required to protect the memory section from being accessed" (claim 1 of the present invention - emphasis added). As explained above, Hasbun instead simply teaches preventing updates to a particular block but still "allowing read access. In particular, refer to Figure 6 of Hasbun showing that no matter what the setting of the "Block Selector" bit, both blocks 1 and 2 of the non-volatile memory are still accessible. Specifically, when the block selector is 1, boot occurs from block l and updates are permitted to block 2. Alternatively, when the block selector is 0, boot occurs from block 2 and updates are permitted to block 1, Applicant notes that read access must be enabled for boot to occur and therefore the teachings of Hasbun are not equivalent to the present invention of turning on the address translator utilizing the control signal so that the second logic address data is outputted as the physical address data when it is required to protect the memory section from being accessed" (claim 1 - emphasis added)

Applicant's arguments towards **claims 1-3, 5-11, 13, 15-17 and 19-21** have been considered, but the Examiner respectfully disagrees. The Examiner contends that the boot selector's value still does not permit write access to one of the blocks and thus still

blocking write access to the currently selected block to be read, as evidenced by

Hasbun, column 6, lines 31-50.

With respect to arguments pertaining to claims 4, 12, 14, and 18 on page 10, lines 30-32 which states:

As previously mentioned, claims 4, 12, 14, and 18 are dependent upon claims 1 and 7 believed to be allowable by the applied art for the above-stated reasons. Therefore claims 4, 12, 14, and 18 should be found allowable for at least the same reasons.

Applicant's arguments towards **claims 4, 12, 14, and 18** have been considered, but the Examiner respectfully disagrees for at least the same reasons as above.

With respect to arguments pertaining to claims 4, 12, 14, and 18 on page 10, lines 30-32 which states:

For at least these reasons, applicant asserts that new claim 22 should be found allowable with respect to the cited references. Consideration of new claim 22 is respectfully requested.

Applicant's arguments towards **claims 4, 12, 14, and 18** have been considered, but the Examiner respectfully disagrees for at least the same reasons as above.

5. RELEVANT ART CITED BY THE EXAMINER

The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See **MPEP 707.05(c)**.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references include:

Bedarida (US Patent # 6,049,854), which teaches a system and method for sharing physical memory among distinct computer environments.

6. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. ' 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 1-22 have received a first action on the merits and are subject of a first action non-final.

b. DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prasith Thammavong whose telephone number is (571) 270-1040 can normally be reached on Monday - Thursday 9:00am - 6:00pm and the first Friday of the bi-week, 9:00 am –5:00 pm

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Prasith Thammavong
Patent Examiner
Art Unit 2187
June 6, 2007

DONALD SPARKS
SUPERVISORY PATENT EXAMINER